

UNIVERSAL ASSEMBLER VERSION 3.1 FEBRUARY 29, 1980 (IN-HOUSE)

C O N F I D E N T I A L P R O P R I E T A R Y I N F O R M A T I O N

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COMMAND LINE WAS: SNAP3 PROC14.MLTI,,,PROC144:GBQPLX

INCLUSION A: PROCINC/TXT:DR0
INCLUSION B: PROC14/LIB:DR0.PMACMIC
INCLUSION C: PROC14/LIB:DR0.GMACROZ
INCLUSION D: PROC14/LIB:DR0.PROCEQUS
INCLUSION E: PROC14/LIB:DR0.BDEF1800
INCLUSION F: PROC14/LIB:DR0.MDEF1800
INCLUSION G: PROC14/LIB:DR0.PORTEQUS
INCLUSION H: PROC14/LIB:DR0.PORTASGN
INCLUSION I: PROC14/LIB:DR0.PROCP4

D 20.A

CAPIVS EQU 0

INVERTED DISPLAY SCREEN VERSION **NEW**

*** ERRORS: D

PROGRAM NAME: MLTI

| | | | | |
|-------------------------|--------|------------|-------------|-------|
| PROGRAM ADDRESS BLOCKS: | 010000 | /ABSOLUTE/ | SIZE=000000 | (ABS) |
| | 167400 | /SYSIVR/ | SIZE=000400 | (ABS) |
| | 170000 | /SYSROM/ | SIZE=000047 | (ABS) |
| | 006000 | /CDOXL/ | SIZE=001000 | (ABS) |
| | 000000 | /CDOXP/ | SIZE=002000 | (REL) |

EXTERNAL DEFINITIONS:

| | | | | | | | |
|--------|--------|---------|--------|--------|--------|--------|--------|
| COMMT | 006000 | COMMR | 006114 | RCVMRK | 006202 | INPUT | 006462 |
| PIN | 006477 | EXADR | 006512 | EXSTAT | 006546 | EXDATA | 006563 |
| OUTPUT | 006600 | EXWRITE | 006600 | EXMOUT | 006610 | EXCOM3 | 006634 |
| EXCOM1 | 006665 | EXCOM2 | 006724 | EXCOM4 | 006724 | | |

PAGE 2 PROC14/LIB:DR0.MLT1

MICRO-PROCESSOR MULTIPOINT COMM SUPPORT - HJS -
SATURDAY, AUGUST 7, 1982 -- 3:49:47 PM

07AUG82 15:52

EXTERNAL REFERENCES (UNDEFINED SYMBOLS):

SRVNXT FETCHI FETCH FETCHW SCLSTW IVIOL\$ MEMPF\$

UNUSED LABELS:

PSWND

| | | | | | |
|-----|----------|-----|----|---------|----|
| 1. | . | | | | |
| 2. | . 2.14.I | HJS | 82 | AUG | 7 |
| 3. | . 2.14.G | HJS | 80 | FEB | 26 |
| 4. | . 2.14.F | HJS | 80 | JAN | 16 |
| 5. | . 2.14.E | HJS | 79 | OCT | 16 |
| 6. | . 2.14.D | HJS | 79 | AUG | 30 |
| 7. | . 2.14.C | HJS | 79 | AUG | 20 |
| 8. | . 2.14.B | HJS | 79 | AUG | 14 |
| 9. | . 2.14.A | HJS | 79 | JULY | 31 |
| 10. | . | | | | |
| 11. | . | | | | |
| 12. | * | | | | |
| 13. | | INC | | PROCINC | |

CONVERSION TO NEW MULTI-PORT CODE
 LAST BUG FOUND (I HOPE) - SET RINGING
 CONVERT TO FINAL SYSTEM
 SETUP FOR FIRST TEST RUN
 START TO ADD USER INST. INTERFACE
 SELECT SECOND GENERATION CODE
 TRY SECOND GENERATION TRANSMITTER
 START GENERATION OF IMA
 INTERNAL MULTIPOINT ADAPTER
 (INTERNAL RIM ALSO USES 2.14.A TO G)

DATAPOINT CONFIDENTIAL INFORMATION - SEE PAGE 1

PAGE 4 PROC14/LIB:DR0.MLTI

MICRO-PROCESSOR MULTIPOINT COMM SUPPORT - HJS - 07AUG82 15:52
. UNDEFINED UNUSED PORTS, SUBS, & BITS

14.A
15.A
16.A

| | | | |
|--------|---------|-----------------|---|
| | SNAPOPT | X | |
| * TYPE | EQU | 4 | DEFINE VERSION OF MACHINE TO BE ASSEMBLED |
| | INC | PROC14.PORTASGN | PORT ASSIGNMENT DISPLAY |

MICRO-PROCESSOR MULTI-PORT COMM SUPPORT - HJS - 07AUG82 15:52
 . THE PORT ASSIGNMENTS, ORGANIZED BY PORT - SUBPORT NUMBER IN IN/OUT PAIRS

3.H
4.H
5.H
6.H
7.H
8.H
9.H
10.H
11.H
12.H
13.H
14.H
15.H
16.H
17.H
18.H
19.H
20.H
21.H
22.H
23.H
24.H
25.H
26.H
27.H
28.H
29.H
30.H
31.H
32.H
33.H
34.H
35.H
36.H
37.H
38.H
39.H
40.H
41.H
42.H
43.H
44.H
45.H
46.H
47.H
48.H
49.H
50.H
51.H

```

*
.PORT
. SUB 0 1 2 3 4 5 6 7
. 0 0 LIREG LIMP BASW MODW STW LUF LUCF
. 0 1 MODIN INBUS MIFIN SDLCIN ACUIN
. 0 0 IIMP DIMP COMF CHUF IMAR DMAR
. 10 1
. 1 0 OTBUS MDW LSPKR SDLCOT ACUOT SDLCMD MIFADR MIFDAT
. 0 1 SRVREQ STATUS IDCODL IDCODH UCFLG MDR STEK
. 1 0 MIFSTB MIFIAR MIFSTB2 SINS SIOD CSRF CSTF SOTS
. 10 1
. 2 0 LDCH LDMAP SKCH SDLM KBSC RDLM CMPF SMR
. 0 1 KBDD SNID
. 3 0 URFO
. I
. 4 0 URO (MR2XXL)
. I MARIL
. 5 0 URO (MR2XXH)
. I MARIH
. 6 0 MAROL (XX2MRL)
. I URI
. 7 0 MAROH (XX2MRH)
. I URI
.
. USER IO PORTS 4-7
. REGS 0 URA URB URC URD URE URH URL URX
. 10 PCH PCL SPH SPL PSW I35 I02 IMP
*
.SUBITS 0 1 2 3 4 5 6 7
.
.SRVREQ: SCPMEM SCMBUS SCSDLOR SCSDLCT SCDSPNL SCONMS SCHUMS
.
.STATUS: STUSCF STIODR STPFIN STPFOL STKBKC STKBNS STKBRDY STBOTLN
.
.MODW: SWINTE SWBASD SWUSER SWSTDT SWRPT SWALBT
.
.STEK: STLA STLW STLSP
.

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MICRO-PROCESSOR MULTIPOINT COMM SUPPORT - HJS - 07AUG82 15:52
 . THE PORT ASSIGNMENTS, ORGANIZED BY PORT - SUBPORT NUMBER IN IN/OUT PAIRS

52.H
 53.H
 54.H
 55.H
 56.H
 57.H
 58.H
 59.H
 60.H
 61.H
 62.H
 63.H
 64.H
 65.H
 66.H
 17.A
 1.I 000002
 2.I 000014
 3.I
 4.I 000004
 5.I
 6.I
 7.I
 8.I
 9.I
 10.I
 11.I

*
 . JUMP INPUT CONDITION CODES ARE:
 .
 .SELECT 0 1 2 3 4 5 6 7
 .
 . CARRY ZERO MEMRDY PARITY IMPZERO IMPODD BUSRDY TRUE
 .
 *
 . DOUBLY NAMED (SUB)PORTS ARE:
 .
 . URO <> MR2XXL
 . URO <> MR2XXH
 . MAROL <> XX2MRL
 . MAROH <> XX2MRH
 .
 . INC PROC14.PROCP4 INDIRECT TO PARAMETER FILE
 VER EQU 2 1800 - INFO INSTRUCTION PROCESSOR NUMBER
 REV EQU 014 INFO INST. MICRO-CODE REVISION NUMBER
 .
 . TYPE EQU 4 =0 FOR 1800 PROCESSOR (DISK, ICA)
 . =1 FOR 1871 PROCESSOR (DISK, ICA, APF/AML)
 . =2 FOR 3800 PROCESSOR (ICA)
 . =3 FOR 3802 PROCESSOR (RIM)
 . =4 FOR 38MP PROCESSOR (IMA)
 *
 . SNAPOPT X
 *

| | | | | |
|-------------|--------|---|--------|---|
| 14.I | * | | | |
| 15.I | • | CONDITION CODES | | |
| 16.I | • | | | |
| 17.I 020002 | MO | EQU | F6+2 | MEMORY READY |
| 18.I 020003 | MP | EQU | F6+3 | MEMORY FAILURE (OF ANY SORT!) |
| 19.I 020004 | IZ | EQU | F6+4 | IMPLICIT REGISTER ZERO |
| 20.I 020005 | IO | EQU | F6+5 | IMPLICIT REGISTER ODD |
| 21.I 020006 | BR | EQU | F6+6 | BUS READY (MICRO-BUS ONLY) |
| 22.I | * | | | |
| 23.I | • | REGISTER ALLOCATION | | |
| 24.I | • | | | |
| 25.I 010002 | Q | EQU | F5+02 | NOBODY SHOULD DO WRITE'S TO Q |
| 26.I | • | | | |
| 27.I 010000 | PDLNP | EQU | F5+0 | DISPLAY LINE POINTER |
| 28.I 010001 | KBSCNT | EQU | F5+01 | KEYBOARD SCAN COUNTER |
| 29.I 010002 | SCANSV | EQU | F5+02 | KEYBOARD SAVED SCAN NUMBER, REPEATED AI |
| 30.I | * | | | |
| 31.I | • | DISKETTE CONTROL REGISTERS | | |
| 32.I | • | | | |
| 33.I 010003 | MADR | EQU | F5+03 | DISKETTE DEVICE ADDRESS |
| 34.I 010004 | MBITS | EQU | F5+04 | DISKETTE I/O CONTROL, FUNCTION & STATUS |
| 35.I 010005 | MBSTAT | EQU | F5+05 | DISKETTE STATE CONTROL LINK REGISTER |
| 36.I 010006 | MCRCH | EQU | F5+06 | DISKETTE CRC GENERATOR STORAGE REG. |
| 37.I 010007 | MCRCL | EQU | F5+07 | DISKETTE CRC GENERATOR STORAGE REG. |
| 38.I 010010 | MDSKS | EQU | F5+010 | DISKETTE HEADER READ SECTOR NUMBER |
| 39.I 010011 | MDSKT | EQU | F5+011 | DISKETTE HEADER READ TRACK NUMBER |
| 40.I 010012 | MTRAK | EQU | F5+012 | DISKETTE USER DESIRED TRACK NUMBER |
| 41.I 010013 | MSECT | EQU | F5+013 | DISKETTE USER DESIRED SECTOR NUMBER |
| 42.I | • | | | * APF VERSION ABOVE 2 BYTES IN MEMORY * |
| 43.I | * | | | |
| 44.I | • | HONEYWELL-APF DMA CHANNEL CONTROL REGISTERS | | |
| 45.I | • | | | |
| 46.I 010013 | APFRP | EQU | F5+013 | APF RECEIVER POINTER LSB |
| 47.I 010014 | APFRK | EQU | F5+014 | APF RECEIVER COUNTER LSB |
| 48.I 010015 | APFTP | EQU | F5+015 | APF TRANSMITTER POINTER LSB |
| 49.I 010016 | APFTK | EQU | F5+016 | APF TRANSMITTER COUNTER LSB |
| 50.I | * | | | |
| 51.I | • | AUDIO CHANNEL CONTROL REGISTER | | |
| 52.I | • | | | |
| 53.I 010015 | ACD | EQU | F5+015 | AUDIO CHANNEL ATTEN/VALUE |
| 54.I 010016 | ACPL | EQU | F5+016 | |
| 55.I 010017 | ACPH | EQU | F5+017 | AUDIO CHANNEL CONTROL & MSB POINTER |
| 56.I 010017 | ACCTL | EQU | ACPH | APF - AUDIO CHANNEL 1 BYTE CONTROL |
| 57.I | • | | | (ACPH & ACCTL SHOULD BE SAME REG.) |

```

58.I
59.I
60.I
61.I 030000
62.I 030001
63.I 030002
64.I 030001
65.I 030002
66.I
67.I
68.I
69.I 030003
70.I 030004
71.I 030005
72.I 030006
73.I 030007
74.I 030010
75.I 030011
76.I 030012
77.I 030013
78.I 030014
79.I 030015
80.I 030016
81.I 030017
82.I
83.I
84.I
85.I
86.I 010013
87.I 030003
88.I 030004
89.I 030005
90.I 030006
91.I 030007
92.I 030010
93.I 010014
94.I 030012
95.I 030013
96.I 030014
97.I 030015
98.I 030016
99.I 030017

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*
. TEMPORARIES - AVAILABLE IN ANY ROUTINE, LOST BETWEEN ROUTINES
.
LINK      EQU      F5+F6+00      SUBROUTINE CALL AND RETURN LINKAGE REGS
TEMP1     EQU      F5+F6+01      PROCESSOR EMULATION TEMPORARIES
TEMP2     EQU      F5+F6+02
TEMPH     EQU      TEMP1          H & L ONLY FOR DOUBLE H/L MACROS
TEMPL     EQU      TEMP2
*
. COMMUNICATIONS CHANNEL CONTROL REGISTERS
.
RSTAT     EQU      F5+F6+03      COM RECEIVER STATUS
RPNTR     EQU      F5+F6+04      COM RECEIVER MEMORY POINTER
RDATA     EQU      F5+F6+05      COM RECEIVER DATA
RCRCH     EQU      F5+F6+06      COM RECEIVER CRC GENERATOR STORAGE AREA
RCRCL     EQU      F5+F6+07      COM RECEIVER CRC GENERATOR STORAGE AREA
UXPNTR    EQU      F5+F6+010     USER TRANSMIT BUFFER POINTER
COMMODE   EQU      F5+F6+011     COMMUNICATION MODE CONTROL REGISTER
URPNTR    EQU      F5+F6+012     USER RECEIVE BUFFER POINTER
XSTAT     EQU      F5+F6+013     COM TRANSMITTER STATUS
XPNTR     EQU      F5+F6+014     COM TRANSMITTER MEMORY POINTER
XDATA     EQU      F5+F6+015     COM TRANSMITTER DATA
XCRCH     EQU      F5+F6+016     COM TRANSMITTER CRC GENERATOR STORAGE
XCRCL     EQU      F5+F6+017     COM TRANSMITTER CRC GENERATOR STORAGE
*
. INTERNAL MULTI-PORT ADAPTER CONTROL REGISTER
.
.COMMODE   EQU      F5+F6+011!!!  COMMUNICATIONS MODE
TRNFCN    EQU      F5+013        TX CONTROL LINE SHADOW
TRNCHN    EQU      F5+F6+03      TRANSMITTING CHANNEL NUMBER
TRNDTA    EQU      F5+F6+04      TRANSMITTING CHANNEL DATA
TRNCTL    EQU      F5+F6+05      TRANSMITTING CHANNEL CONTROL
TRNSEL    EQU      F5+F6+06      TRANSMITTING CHANNEL SELECTION
RCVCTL    EQU      F5+F6+07      RECEIVER CONTROL REGISTER
RCH0C     EQU      F5+F6+010     SWAP OUT WITH COMMODE
RCH0D     EQU      F5+014
RCH1C     EQU      F5+F6+012
RCH1D     EQU      F5+F6+013
RCH2C     EQU      F5+F6+014     RECEIVER CHANNEL & DATA REGISTERS
RCH2D     EQU      F5+F6+015
RCH3C     EQU      F5+F6+016
RCH3D     EQU      F5+F6+017

```



```

100.I
101.I
102.I
103.I
104.I
105.I
106.I
107.I
108.I
109.I
110.I
111.I
112.I
113.I
114.I
115.I 000000
116.I 000002
117.I 000000
118.I 000000
119.I 000000
120.I 000000
121.I 000100
122.I 000000
123.I
124.I
125.I 000102
126.I
127.I
128.I
129.I 000000
130.I 002000
131.I 004000
132.I 006000
133.I 007000
134.I
135.I 000000
18.A 000111
19.A
D 20.A 000000
21.A

```

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*
. CAPABILITY BITS:
. THESE BITS DEFINE THE VERSION OF THE 1800/3800 PROCESSOR THAT THIS IS FOR
.
. XX XXX XXX
.      0 --- MICRO I/O BUS AVAILABLE
.      1 ---- 1500 SINGLE DENSITY DISKETTE DRIVE AVAILABLE
.      2 ----- 1800 SINGLE/DOUBLE DISKETTE DRIVE AVAILABLE
.      3 ----- APF SPECIAL MICRO-BUS INTERFACE AVAILABLE
.      4 ----- INTERNAL MULTIPOINT ADAPTER AVAILABLE
.      5 ----- INBOARD RIM AVAILABLE
.      6 ----- 5500 I/O BUS AVAILABLE
.      7 ----- COMMUNICATIONS INTERFACE AVAILABLE (ASYN, BISYN, & SDLC)
.
. *PROCESSOR*
CAPMICR EQU 0<0 YES YES
CAPIMA EQU 1<1 YES YES
CAPBLUE EQU 0<2 YES YES
CAPAPF EQU 0<3 YES
CAPDMPIO EQU 0<4 YES
CAPRIM EQU 0<5 YES
CAP55IO EQU 1<6 YES YES YES YES
CAPCOM EQU 0<7 YES YES YES
. *TYPE*
0 1 2 3 4
CAPABILI EQU CAPCOM+CAP55IO+CAPRIM+CAPDMPIO+CAPAPF+CAPBLUE+CAPIMA+CAPMICR
*
. LOCATION OF THE CODE IN ROMS IS AS FOLLOWS (MSB & LSB OF COURSE)
.
PROC EQU 00<9 EMULATION SUPPORT CODE IN ROMS 0 & 1
PROD EQU 02<9 EMULATION SUPPORT CODE IN ROMS 2 & 3
FLEX EQU 04<9 MICRO-BUS CODE IN ROMS 4 & 5
CDOX EQU 06<9 COMM TRANSMIT CODE IN ROM 6
CDOR EQU 07<9 COMM RECEIVE CODE IN ROM 7
.
CAPIVS EQU 0
PRE EQU '1'
RELEASE LEVEL (FINAL IS BINARY ZERO)
*
CAPIVS EQU 0
INVERTED DISPLAY SCREEN VERSION **NEW**
0 = NORMAL, 1 = INVERTED (PURE RASTER!)

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16.      *
17. 000151 IMAADR EQU 0151 ADDRESS OF THE 9462 BEING REPLACED
18.      *
19.      . CPU DATA LOGICAL "1" "0"
20.      . RS232C/RS363 DEFINES MARK, -VE SPACE, +VE
21.      . TRANSMITTER (4800 BAUD) MARK SPACE
22.      . RECEIVER!!!! (300 BAUD) SPACE, TC MARK, FC
23.      . ** NOTE: RECEIVER INVERSION ** (ACUIN LINES INVERTED ON INPUT!)
24.      *
25.      . RECEIVER TRANSITION (x) & SAMPLE (v) POINTS
26.      . ...x= = = =v= = = =x= = = =v= = = =x= = = =v= = = =x...
27.      . CLOCK: 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
28.      . 1-----1 DELTA/2 1---DELTA = 8---1
29.
30. 000010 DELTA EQU 8 DELAY COUNT SAMPLE INTERVAL
31. 000140 TCOUNT EQU 16-8-2<4 8 DATA & 2 STOP BITS IN THE 4 BIT COUNTER
32.      *
33.      . CONTROL REGISTERS INTERNAL DEFINITIONS:
34.      . RCVCTL 3'2'1'0'3 2 1 0 0..3 RECEIVER READY (WIH DATA)
35.      . 0'..3' RECEIVER ERROR BITS (BREAK!)
36.      . TRNCTL Z Z Z Z 3 2 1 0 0..3 TRANSMITTER READY STATUS
37.      . ZZZZ ALWAYS ZERO
38.      . TRNSEL K K K K 3 2 1 0 0..3 TRANSMITTER PORT SELECTED FOR OUTPUT
39.      . KKKK COUNTER OF BITS GOING OUT
40.      . TRNCHN Z Z Z Z 3 2 1 0 0..3 TRANSMITTER CHANNEL DATA (SPACE/MARK)
41.      . TRNDTA & RCHXD D D D D D D D D DATA BEING SHIFTED OUT AND IN
42.      . RCHXC ^ U U U U U U U U MICRO-ADDRESS FOR RECEIVER CONTROL
43.      . ^X^ & ^X^ X VARIES FROM 0 TO 3 (PER CHANNEL REGS)
44.      . TRNCTL & TRNCHN NOTE: ONLY 1 BIT MAY BE SET (1 CHANNEL)
45.      . TRNFCN A X X 2 3 X 1 0 0..3 TRANSMITTER DTR
46.      . A = 1 WHEN MULTI-PORT COMES ALIVE
47.
48.      . COMMODE Z Z E X 3 2 1 0 Z ALWAYS ZERO ** ONLY 1 BIT MAY BE 1**
49. 000040 COMMNPS EQU B5 E DEVICE ADDRESSED NO PORT SELECTED YET
50. 000020 COMMNXP EQU B4 X EXTRA (NON-PORT) 4-7 SELECTED
51. 000017 COMMPTS EQU B3+B2+B1+B0 3..0 EX ADR & EX COM3 SELECTED PORT
52.      *
53.      . INTERNAL MULTI-PORT ALLOCATION OF COMMAND STROBES ON AVAILABLE CONTROL BITS
54.      .
55.      . ACUIN 0 0 5 4 3 2 1 0 3..0 RECEIVER DATA FOR CHANNEL 3..0
56.      . 4 RECEIVER 2 CLEAR TO SEND (DSR/CD...)
57.      . 5 RECEIVER 3 CLEAR TO SEND (DSR/CD...)
58.      . MODIN 0 6 1 4 1 0 0 0 1'S MASTER CD & CTS MUST BE ONE'S
59.      . 4 RECEIVER 0 CLEAR TO SEND (DSR/CD...)
60.      . 6 RECEIVER 1 CLEAR TO SEND (DSR/CD...)
61.      . MODOUT X X X 0 3 X 1 1 1'S MASTER DTR & RTS MUST BE ONE'S
62.      . 3 (NEW SYNC) CAN BE ANYTHING
63.      . 0 MASTER SET BRAKE MUST BE ZERO
64.      . ACUOT X X 5 4 3 2 1 0 3..0 TRANSMITTER OUTPUT FOR CHANNEL 3..0
65.      . 4 (DIGIT PRESENT = 0)
66.      . 5 (CALL REQUEST = 0)
67.      . SDLCIN ? ? ? ? ? ? ? 0 0 MASTER RECEIVE DATA (IGNORED)

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68. . SDLCOT          X X X X X X X 0 0  MASTER TRANS. (MATCHES CHANNEL 0)
69. . SDLCMD          X X X 2 3 X 1 0  3..0 DTR FOR CHANNELS 3..0
70.
71. 000350
72. *
73. .MACRO.           MACRO
74. .MACRO.           RECEIVE CHN
75. .MACRO.           BAL LINK,RCHICHNIEND SET RETURN ADDRESS FOR ROUTINE CALL
76. .MACRO.           LDRI TEMP2,CHN SET CHANNEL NUMBER FOR THE ROUTINE
77. .MACRO.           LDRR TEMP1,RCHICHNID,CC LOAD CHANNEL DATA FOR CHANNEL IN USE
78. .MACRO.           DOTPI ,ND,ACUIN,1<CHN GET CHANNEL'S MARK/SPACE BIT
79. .MACRO.           DOTI ,AC,0377 SET CARRY ON MARK!
80. .MACRO.           BRR RCHICHNIC GO TO THE CONTROL ROUTINE
81. .MACRO.           RCHICHNIEND BAS RCHICHNIC SAVE THE STATE FOR NEXT TIME
82. .MACRO.           LDRR RCHICHNID,TEMP1 SAVE THE NEW DATA TOO
83. .MACRO.           MEND
84.
85. .MACRO.           MACRO
86. .MACRO.           BIT2ADR ADDRESS 850 NSEC WORST CASE
87. .MACRO.           TSTIT ,014
88. .MACRO.           BRA BITOK,TZ WAS 0001(1) OR 0010(2) - LEAVE AS IS
89. .MACRO.           DOTI ,SB,1
90. .MACRO.           TSTIT ,014
91. .MACRO.           BRA BITOK,TZ WAS 0100 - CHANGED TO 0011(3)
92. .MACRO.           LDTI 4 WAS 1000 - CHANGED TO 0100(4)
93. .MACRO.           BITOK DOPI MAROL,AC,ADDRESS NOW INDEX INTO MEMORY BY BIT POSITION
94. .MACRO.           MEND
95.

```

| | | | |
|---|---------------------------------|--|--|
| * CDOXL CDOXP CDOXL CDOXP * COMMT: . 400 | ORG ORG USE USE LOC | CDOX 0 CDOXL CDOXP CDOXL,2 | |
| | | | !!!ALL TIMINGS WORST CASE !! |
| | LDTR BRA TSTIT BRA | TRNSEL,CC SENANY,TZ ,0360 SENDTA,FZ | CHANNELS ALIVE? IF NONE, TRY SOME AT THE START? NO, JUST DO NEXT DATA BIT |
| . SENSTRT . 2400 | | | |
| | MWAIT | ,MEMPF6 | |
| . | LDTR BIT2ADR | TRNSEL,CC SVCTRN-1 | CONVERT BIT TO NUMBER GET TRANSMITTER DATA BYTE (ORIGIN 1 FIX) |
| | | | |
| | LDPI | MAROH,SVCTRN>8 | MSB OF DATA ADDRESS |
| | DOPIP | MODW,ND,-1-SWUSER,PSWI | |
| | STB DORIR | SMR TRNSEL,OR,TCOUNT,TRNSEL,CC | INIT COUNTER WITH 2 STOP BITS |
| | DOTI DOTI DORR | ,ND,017 ,XR,0377 TRNCTL,ND,TRNCTL | HAVE 1 1 1 1 X X X X (ONLY ONE "X" IS A 0) TO TURN OFF BIT FOR CHANNEL TRANSMITTING |
| | MWAIT | ,MEMPF6 | |
| | LDRP | TRNDTA,MDR | GET DATA & OUTPUT ITS FIRST BIT |

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125.
126. 006037L
127.
128. 006037L 01010001 00000001
129. 006040L 01110001 10110100
130. 006041L 00010111 10010010
131. 006042L 01101111 11110100
132. 006043L 00010111 10010010
133. 006044L 01010101 10000000
134. 006045L 11000010 11011000
135. 006046L 01110001 11110110
136. 006047L
137.
138.
139.
140.
141.
142.
143. 006047L 01010011 00110000
144. 006050L 01010000 00001111
    006051L 01101111 11110011
145. 006052L 01110001 10110110
    006053L 01010010 00010000
    006054L 01101111 11110110
146. >006055L 01011001 11111111
    >006056L 11000000 11111111
147. 006057L 01011001 11110011
148.
149.
150.
151.
152.
153.
154. 006060L 01110001 11110110
    006061L 01101111 11110001
155. 006062L 01110001 11110101
156. 006063L 11000011 10111001
157.
158.
159.
160.
161.
162.
163.
164.
165.
166.
167. 006064L 01010001 11001001
    006065L 11001111 11000010
167. 006066L 01010001 11000111
    006067L 11001111 11000010
168. 006070L 01010001 10111001

```

```

*
SENDA
. 800

```

```

LDTI      I          SET LINK TO SHIFT IN 1
LDTR      TRNDTA,CC   FOR THE TWO STOP BITS
SHIFT     SR          SHIFT NEXT DATA BIT TO LINK
LDRT      TRNDTA
SHIFT     SR
TSTIT     ,0200,..,TW MARK OR SPACE?
BRA       SENMARK,FZ  ON MARK: T-REG = 0200; ON SPACE: T = 0
LDTR      TRNSEL      SEND A SPACE (ONE CHANNEL ONLY!)
                        SENDING A MARK (T MUST BE CORRECT, ZERO!)

```

SENMARK

* *RE-DO SO THAT:

- . IF ANY "OTHER" CHANNEL IS AVAILABLE FOR TRANSMISSION, SWITCH
- . TO IT BEFORE SENDING STOP BITS ON PRESENT CHANNEL.
- . THIS WILL ENABLE HIGHER EFFECTIVE SPEED BY HIDING BOTH STOP BITS
- . BEHIND ANOTHER CHANNELS DATA TRANSMISSION.
- . 900

```

DOTI      ,OR,B5+B4   SET COMM ALIVE BITS
DORI      TRNCHN,XR,017 SAVE CHANNEL BITS FOR NEXT INTERRUPT
DORIR     TRNSEL,AC,1<4,TRNSEL,CC
BRAX      SRVNXT,FC    CONTINUE TILL COUNTER OVERFLOWS
BPGX      $           REACHED THE END, DO THE NEXT

```

```

*
. SENEXT
.

```

- . FIND NEXT FREE CHANNEL TO GET DATA FROM
- . SEARCH IS DONE IN A ROUND ROBIN FASHION
- . 400

```

LDRR      TEMP1,TRNSEL SET STARTING TEST POINT

```

```

SENTRY    LDTR      TRNCTL      (SPEEDUP IF NOTHING TO DO)
          BRA       SENEND,TZ   YES, I HAVE NO BANANAS

```

- . NOTE: IN THE FOLLOWING REPEATS THERE ARE ONLY "3" TOTAL NOT 4.
- . THIS IS SO THAT THE TRAILING MARK OF A CHANNEL JUST COMPLETED
- . CAN OVERLAP THE LEADING SPACE OF THE NEXT CHANNEL.
- . WHY THREE? BECAUSE IT CAN NOT OVERLAP ITSELF!
- . THIS WILL INSURE TWO FULL STOP BITS BEFORE THE START BIT OF
- . THE SAME CHANNEL BEING FINISHED & SELECTED AS NEXT.
- . TCOUNT MUST BE SET CORRECTLY TO DO THIS! ** NOT SO AT PRESENT **
- . 2*1300+1300+600

```

RPT       (4-1)-1      4-1 PORTS IN ROUND ROBIN
BRC       CHKNXT

```

```

BRC       CHKNXT

```

```

BRC       CHKNXT,,SENEND LEAVE MARKING IF NO AVAILABLE DATA FOUND

```

```

169. 006071L 11001111 11000010
170. 006072L 01010001 11001101
    006073L 01101111 11110000
    006074L 11001111 10111101
171.
172.
173. 006075L
174.
175.
176.
177. 006075L 01101111 11110000
178. 006076L 01110001 11110001
179. 006077L 00010111 10100010
180. 006100L 01010101 00001110
181. 006101L 11000010 10111100
182. 006102L 01010001 00000001
183. 006103L 01101111 11110001
184. 006104L 01110101 11110101
185. 006105L 11110001 00000000
186. 006106L 01101111 11110110
187. 006107L 01010011 00110000
188. 006110L 01010000 00001111
    006111L 01101111 11110011
189. >006112L 01011001 11111111
    >006113L 11001111 11111111

```

```

*
SENANY  BRS      CHKANY,,SENTRY  DO FOUR STEPS IF QUIET BEFOREHAND

. 400+500
*
CHKNXT

. CHECK IF CHANNEL AS SPECIFIED BY TEMPI CONTAINS DATA TO BE OUTPUT
.
      BAS      LINK      SAVE RETURN ADDRESS
      LDTR     TEMPI
      SHIFT    SL        CHECK THE NEXT CHANNEL IN SEQUENCE
      DOTI     ,ND,07<1  HIGH BITS SHIFT IN ZERO
      BRA      CHKCHN,FZ
CHKANY  LDTR     1<0      TRY CHANNEL 0 AFTER 3
CHKCHN  LDRT     TEMPI   SAVE CHANNEL MARKER
      DOTR     ,ND,TRNCTL IS THERE DATA? (T = 0 FOR LAST BRC)
      BRR      LINK,TZ   NOT ON THIS ONE
SENEND  LDRT     TRNSEL   SAVE SELECTED CHANNEL'S BIT MARKER
      DOTI     ,OR,B5+B4  SET COMM ALIVE BITS
      DORI     TRNCHN,XR,017 SEND THE LEADING SPACE (OR MORE MARKS!)

      BRAX     SRVNXT

. TRANSMITTER TIMINGS RESULTS:
.      NOTHING TO DO      1700
.      AVERAGE PER BIT   2200
.      FIRST BIT SPECIAL  5200
.      LAST BIT WORST CASE 7200 (SAME CHANNEL READY BUT NO OTHERS)

```

196.
 197. 006114L

+
 COMMR:

198.
 199.
 200.
 201.
 202.
 203.
 204.
 205.
 206.

. RECEIVER TIMINGS RESULTS:
 . 4*1450+300+4*3100 = 18500 NSEC
 . 4 CHANNELS TO BE EXAMINED
 . 300 NS RETRUN TO SERVICE REQUEST CONTROL
 . 4 CHANNELS WORST CASE (ALL FINISHED CHARACTER AT SAME TIME)
 .
 . AVERAGE CASE: 4*(1450+300)+300 ALL CHANNELS DOING BRRC DELAY COUNTING

207. 006114L 01010001 10101001
 006115L 01101111 11110000
 006116L 01010001 00000000
 006117L 01101111 11110010
 006120L 00010001 10111100
 006121L 01101111 10110001
 006122L 01010001 00000001
 006123L 00110101 00010111
 006124L 01010010 11111111
 006125L 11101111 00001000
 006126L 01101111 11111000
 006127L 01110001 11110001
 006130L 00000111 11111100

LDI (251) RECEIVE 0
 BAS LINK
 LDI 0
 LDRT TEMP2
 LDTR RCH0D, 3CC
 LDAT TEMP2, CC
 LDI 1
 DOTP ,ND, AC4IN
 DDI ,AC, 0377
 BR RACH0C
 LDAT RCH0C
 LDTR TEMP2
 LDTR RCH0D

RECEIVE CHANNEL 0

LINK 0
 TEMP2 02
 RCH0D 14
 TEMP1 1
 RCH0C 10
 RCH1D 13
 RCH1C 12

208. 006131L 01010001 10011100
 006132L 01101111 11110000
 006133L 01010001 00000001
 006134L 01101111 11110010
 006135L 01110001 10111011
 006136L 01101111 10110001
 006137L 01010001 00000010
 006140L 00110101 00010111
 006141L 01010010 11111111
 006142L 11101111 00001010
 006143L 01101111 11111010
 006144L 01110001 11110001
 006145L 01101111 11111011

LDI (234) RECEIVE 1
 LDI 1
 LDTR RCH1D
 LDI 2
 BR RCH1C
 LDAT RCH0D

RECEIVE CHANNEL 1

209. 006146L 01010001 10001111
 006147L 01101111 11110000
 006150L 01010001 00000010
 006151L 01101111 11110010
 006152L 01110001 10111101
 006153L 01101111 10110001
 006154L 01010001 00000100
 006155L 00110101 00010111
 006156L 01010010 11111111
 006157L 11101111 00001100
 006160L 01101111 11111100
 006161L 01110001 11110001
 006162L 01101111 11111101

RECEIVE 2

RECEIVE CHANNEL 2

210. 006163L 01010001 10000010
 006164L 01101111 11110000

RECEIVE 3

RECEIVE CHANNEL 3

| | | | |
|------|---------|----------|----------|
| 212. | | | |
| 213. | 006202L | | |
| 214. | 006202L | 01010001 | 01111101 |
| | 006203L | 11100001 | 00000000 |
| 215. | 006204L | 01010001 | 01111011 |
| | 006205L | 11100000 | 00000000 |
| 216. | | | |
| 217. | | | |
| 218. | | | |
| 219. | | | |
| 220. | 006206L | 01010001 | 01110111 |
| | 006207L | 11100001 | 00000000 |
| 220. | 006210L | 01010001 | 01110101 |
| | 006211L | 11100001 | 00000000 |
| 220. | 006212L | 01010001 | 01110011 |
| | 006213L | 11100001 | 00000000 |
| 221. | 006214L | 01010001 | 01111101 |
| | 006215L | 11100000 | 00000000 |
| 222. | | | |
| 223. | | | |
| 224. | 006216L | 01010001 | 10000000 |
| | 006217L | 01101111 | 11110001 |
| 225. | | | |
| 226. | | | |
| 227. | 006220L | 01010001 | 01101101 |
| | 006221L | 11101111 | 00000000 |
| 227. | 006222L | 01010001 | 01101011 |
| | 006223L | 11101111 | 00000000 |
| 227. | 006224L | 01010001 | 01101001 |
| | 006225L | 11101111 | 00000000 |
| 227. | 006226L | 01010001 | 01100111 |
| | 006227L | 11101111 | 00000000 |
| 227. | 006230L | 01010001 | 01100101 |
| | 006231L | 11101111 | 00000000 |
| 227. | 006232L | 01010001 | 01100011 |
| | 006233L | 11101111 | 00000000 |
| 227. | 006234L | 01010001 | 01100001 |
| | 006235L | 11101111 | 00000000 |
| 228. | | | |

*
RCVMRK:
LDTI 0175 BRRC
BAR LNPK, TC
RCVSPC BRRC
BAR LNPK, FC

BRAX SRVNXT

AND DONE!

**** WAITING FOR START (SPACE)
JUST WAIT UNTIL SPACE ENDS**

JUST WAIT UNTIL SPACE RESTARTS

THIS FORCES LEADING EDGE OF SPACE
AS CONDITION FOR START BIT

**** DELAY TILL EARLY MID BIT WHILE SPACING
NEXT STATE ONLY WHILE STILL SPACING**

NEXT STATE ONLY WHILE STILL SPACING

NEXT STATE ONLY WHILE STILL SPACING

IF MARK, THEN START OVER AGAIN

THE DELTA/2 CYCLE (MID START BIT)

LDRI TEMP1.0200

INIT REG TO RECEIVE DATA

WHEN 0200 BIT SHIFTS OUT, GOT ALL DATA
DELAY TILL MID DATA BIT

| | | |
|----------|------|---------|
| RCV DATA | RPT | DELTA-1 |
| | BRRC | LINK |

1 BRRC LINK

7 BRRC LINK

BRRC LINK

4 BRRC LINK

7 BRRC LINK

6 BRRC LINK

| | | | |
|------|---------|----------|----------|
| 229. | | | |
| 230. | | | |
| 231. | 006236L | 01010001 | 00000001 |
| | 006237L | 01010010 | 00000000 |
| 232. | | | |
| 233. | 006240L | 01110001 | 10110001 |
| 234. | 006241L | 00010111 | 10010010 |
| 235. | 006242L | 01101111 | 11110001 |
| 236. | 006243L | 00010111 | 10010010 |
| 237. | 006244L | 01000010 | 10000000 |
| 238. | 006245L | 01010001 | 01101111 |
| | 006246L | 11100000 | 00000000 |
| 239. | | | |
| 240. | | | |
| 241. | 006247L | 01010001 | 01010110 |
| | 006250L | 11101111 | 00000000 |
| 241. | 006251L | 01010001 | 01010100 |
| | 006252L | 11101111 | 00000000 |
| 241. | 006253L | 01010001 | 01010010 |
| | 006254L | 11101111 | 00000000 |
| 241. | 006255L | 01010001 | 01010000 |
| | 006256L | 11101111 | 00000000 |
| 241. | 006257L | 01010001 | 01001110 |
| | 006260L | 11101111 | 00000000 |
| 241. | 006261L | 01010001 | 01001100 |
| | 006262L | 11101111 | 00000000 |
| 241. | 006263L | 01010001 | 01001010 |
| | 006264L | 11101111 | 00000000 |
| 242. | | | |
| 243. | | | |
| 244. | | | |
| 245. | 006265L | 11000100 | 01001010 |
| | 006266L | 11010111 | 00010001 |
| 246. | 006267L | 00110001 | 11011100 |
| | 006270L | 01010101 | 11111011 |
| | 006271L | 00110111 | 00000100 |
| 247. | 006272L | 01010001 | 11101111 |
| | 006273L | 00110111 | 11100000 |
| 248. | 006274L | 01010001 | 01010100 |
| | 006275L | 01110011 | 11110010 |
| | 006276L | 00110111 | 11000000 |
| 249. | 006277L | 01110001 | 11110001 |
| | 006300L | 00110111 | 00100001 |
| 250. | | | |
| 251. | 006301L | 01010001 | 00110100 |
| 252. | 006302L | 01110010 | 10110010 |
| | 006303L | 01101111 | 11110010 |
| 253. | 006304L | 01010001 | 00000001 |
| 254. | 006305L | 11000000 | 00111000 |
| 255. | 006306L | 01010001 | 00010001 |
| 256. | 006307L | | |
| 257. | | | |

| | | |
|---------------|---------------------------------------|---|
| • | THE DELTA CYCLE TO MID DATA BIT | |
| • | DOTII ,AC,0,1 | RECEIVED DATA (IN CARRY) PUT IN BIT 0 TC = SPACE = "0" -> BO = 0 |
| • | | FC = MARK = "1" -> BO = 1 |
| | LDTR TEMPI,CC | GET OLD DATA & PUT NEW BIT INTO THE LINK |
| | SHIFT SR,CC | SHIFT THE DATA IN (DONE BIT TO LINK?) |
| | LDRT TEMPI | |
| | SHIFT SR | GET THE END MARKER BIT (MAYBE?) |
| | TSTIT AC,0200 | SET CARRY IF REACHED THE END |
| | BRRCLINK,FC,RCVDATA | NOT YET, KEEP GOING |
| • | | |
| | RPT DELTA | ** DELAY TILL MID STOP BIT |
| | 0 BRRCLINK | (RECEIVER ACCEPTS 1 STOP BIT!) |
| | 1 BRRCLINK | (RECEIVER ACCEPTS 1 STOP BIT!) |
| | 2 BRRCLINK | (RECEIVER ACCEPTS 1 STOP BIT!) |
| | 3 BRRCLINK | (RECEIVER ACCEPTS 1 STOP BIT!) |
| | 4 BRRCLINK | (RECEIVER ACCEPTS 1 STOP BIT!) |
| | 5 BRRCLINK | (RECEIVER ACCEPTS 1 STOP BIT!) |
| | 6 BRRCLINK | (RECEIVER ACCEPTS 1 STOP BIT!) |
| * | BAC LINK | |
| • | THE DELTA CYCLE TO MID FIRST STOP BIT | |
| • 2050 | MWAIT ,MEMPF6 | |
| | DOPIP MODW,ND,-1-SWUSER,PSWI | |
| | LDPI MAROH,SVCRCV>8 | 167 ^u LOAD ADDRESS OF DATA SAVE AREA |
| | DOPRI MAROL,OR,TEMP2,SVCRCV | 224 SELECT BUFFER LOC. (CARRY HELD!) |
| | LDPR MDW,TEMP1 | STORE DATA (TEMP1 FREE REG NOW!) |
| 64 2 66 | LDTA RCVSTB | SETUP FOR SHIFTS TO BIT POSITION |
| | DORR TEMP2,AC,TEMP2,,HC | BUT, DO NOT CHANGE CARRY!! |
| | LDTI 1<0 | MARK = FC, ASSUMED DATA RECEIVED OK |
| | BRA RCVBRK,FC | (CARRY MUST NOT BE DISTURBED TILL HERE) |
| | LDTI (1<4)+(1<0) | SPACE = TC, DATA RECEIVED ERROR (BREAK?) |
| RCVBRK | | |
| • 200-500 | | |

PAGE 18 PROC14/LIB:DR0.MLTI

MICRO-PROCESSOR MULTI-PORT COMM SUPPORT - HJS - 07AUG82 15:52
 . INTERNAL MULTI-PORT ADAPTER RECEIVER/TRANSMITTER CHANNEL OPERATING CODE

| | | | | | | |
|------|---------|----------|----------|--------|------------------|--|
| 258. | 006307L | 11101111 | 00000010 | BRR | TEMP2 | NOW SHIFT BITS TO CORRECT POSITION |
| 259. | | | | RPT | 4-1 | |
| 260. | 006310L | 00010111 | 10100010 | SHIFT | SL | |
| 260. | 006311L | 00010111 | 10100010 | SHIFT | SL | |
| 260. | 006312L | 00010111 | 10100010 | SHIFT | SL | |
| 261. | 006313L | | | RCVSTB | | FOR 0, IN CORRECT POSITION ALREADY |
| 262. | | | | . 700 | | |
| 263. | | | | IFNE | \$>8,COMMT>8 | |
| 265. | | | | XIF | | |
| 266. | 006313L | 01110011 | 11110111 | DORR | RCVCTL,OR,RCVCTL | SET STATUS BITS AS NEEDED |
| | 006314L | 01101111 | 11110111 | | | |
| 267. | 006315L | 11000100 | 00110010 | MWAIT | ,MEMPF6 | |
| | 006316L | 11010111 | 00010001 | | | |
| 268. | 006317L | 01010001 | 01111101 | BRRC | LINK,,RCVMRK | ANYWAY, FINISHED A CHARACTER SO START OVER |
| | 006320L | 11101111 | 00000000 | | | |

Noop
Noop

AD 2

for future debugging

| | | | | | | |
|------|----------|----------|----------|----------|-------|-------------------------|
| 271. | | | | | | |
| 272. | 006321L | 01010101 | 00010000 | IMAIN | DOTI | ,ND,SWSTD |
| 273. | 006322L | 11010010 | 11101011 | | BRA | IMARDTA,FZ |
| 274. | 006323L | 01101111 | 11110001 | | LDRT | TEMP1 |
| 275. | 006324L | 01110001 | 11111001 | | TSTIR | ,COMMNPS+COMMXP,COMMODE |
| | 006325L | 01000101 | 00110000 | | | |
| 276. | 006326L | 11000010 | 00000001 | | BRA | IMASCOM,FZ |
| 277. | 006327L | 01110101 | 11000101 | | TSTRT | ,TRNCTL |
| 278. | 006330L | 11000010 | 00100011 | | BRA | IMASB0,FZ |
| 279. | 006331L | 01010001 | 00000001 | | LDRI | TEMP1,B0 |
| | 006332L | 01101111 | 11110001 | | | |
| 280. | 006333L | 01110001 | 11111001 | | LDTR | COMMODE |
| 281. | 006334L | | | IMASB0 | | |
| 282. | 006334L | 01110101 | 11000111 | | TSTRT | ,RCVCTL |
| 283. | 006335L | 11000011 | 00010110 | | BRA | IMASB1,TZ |
| 284. | | | | | RPT | 4 |
| 285. | 006336L | 00010111 | 10100010 | | SHIFT | SL |
| 285. | 006337L | 00010111 | 10100010 | | SHIFT | SL |
| 285. | 006340L | 00010111 | 10100010 | | SHIFT | SL |
| 285. | 006341L | 00010111 | 10100010 | | SHIFT | SL |
| 286. | 006342L | 01110101 | 11110111 | | DOTR | ,ND,RCVCTL |
| 287. | 006343L | 11000011 | 00011010 | | BRA | IMASB2,TZ |
| 288. | 006344L | 01010001 | 00000100 | | LDTI | B2 |
| 289. | 006345L | 01010011 | 00000010 | IMASB2 | DOTI | ,OR,B1 |
| 290. | 006346L | 01110011 | 11110001 | | DORR | TEMP1,OR,TEMP1 |
| | 006347L | 01101111 | 11110001 | | | |
| 291. | 006350L | 01110001 | 11111001 | | LDTR | COMMODE |
| 292. | 006351L | | | IMASB1 | | |
| 293. | 006351L | 01000101 | 00001100 | | TSTIT | ,B3+B2 |
| 294. | 006352L | 11000010 | 00001010 | | BRA | IMASBP32,FZ |
| 295. | 006353L | 01000101 | 00000010 | | TSTIT | ,B1 |
| 296. | 006354L | 11000010 | 00001110 | | BRA | IMASBP1,FZ |
| 297. | | | | | | |
| 298. | 006355L | 01010001 | 00010000 | | TSTPI | ,MODIN,B4 |
| | 006356L | 00110101 | 00010000 | | | |
| 299. | 006357L | 11000010 | 00000110 | | BRA | IMASBSTS,FZ |
| 300. | 006360L | 11001111 | 00000101 | | BRA | IMASORZ |
| 301. | 006361L | 01010001 | 01000000 | IMASBP1 | TSTPI | ,MODIN,B6 |
| | 006362L | 00110101 | 00010000 | | | |
| 302. | 006363L | 11000010 | 00000110 | | BRA | IMASBSTS,FZ |
| 303. | 006364L | 11001111 | 00000101 | | BRA | IMASORZ |
| 304. | 006365L | 00010111 | 10100010 | IMASBP32 | SHIFT | SL |
| 305. | 006366L | 00010111 | 10100010 | | SHIFT | SL |
| 306. | 006367L | 00110101 | 00010111 | | TSTPT | ,ACUIN |
| 307. | 006370L | 11000011 | 00000101 | | BRA | IMASORZ,TZ |
| 308. | | | | | | |
| 309. | 006371L | 01010001 | 11101000 | IMASBSTS | LDTI | IMASTS |
| 310. | 006372L | 01110011 | 11110001 | IMASORZ | DOPR | IMPO,OR,TEMP1 |
| | 006373L | 00110111 | 10001111 | | | |
| 311. | >006374L | 01011001 | 11111111 | | BRAX | FETCHI |
| | >006375L | 11001111 | 11111111 | | | |

WAS I IN STATUS OR DATA MODE?

DATA INPUT

INIT STATUS IS ZERO

,COMMNPS+COMMXP,COMMODE

TESTING NON-SELECTED/EXISTANT PORT

SET TRANSMITTER READY BIT

RELOAD PORT SELECT BIT

RECEIVER NOT READY

GET TO ERROR BIT POSITIONS

SEE IF ERROR BIT SET

YES, INCLUDE IT IN BITS SET

COMBINE READY WITH (MAYBE) THE ERROR BIT

SET RECEIVER & BREAK DETECTED BITS AS NEED

RELOAD PORT SELECT BIT

WHICH PORT IS THIS FOR?

PORTS 3 & 2

PORT 0 DSR/CD/RD/CTS SET?

YES

NO

PORT 1 DSR/CD/RD/CTS SET?

YES

NO

P: 3,2 DSR/CD/RD/CTS SET?

NO

RETURN THE GENERATED STATUS

NOP in loop

| | | | | | | | |
|------|---------|----------|----------|---------|---------|------------------------|--|
| 312. | | | | | | | |
| 313. | 006376L | 01010101 | 00100000 | IMASCOM | DOTI | ,ND,COMMNPS | NO PORT SELECTED? |
| 314. | 006377L | 11000011 | 00000101 | | BRA | IMASORZ,TZ | NO. WAS TO NON-EXISTANT PORT |
| 315. | 006400L | 01010001 | 00001111 | | TSTRI | XR,TRNCTL,COMMPTS | ANY AVAIL. PORT WILL BECOME A 1 |
| | 006401L | 01110000 | 11000101 | | | | |
| 316. | 006402L | 11010011 | 11111010 | | BRA | IMASCO,TZ | IF ANY TRANSMITTER AVAILABLE |
| 317. | 006403L | 01010001 | 00000001 | | LDRI | TEMP1,B0 | SET TRANSMITTER READY BIT |
| | 006404L | 01101111 | 11110001 | | | | |
| 318. | 006405L | | | IMASCO | | | |
| 319. | 006405L | 01110001 | 11110111 | | LDTR | RCVCTL | |
| 320. | 006406L | 11010011 | 11110010 | | BRA | IMASC1,TZ | NO RECEIVER IS READY |
| 321. | 006407L | 01010101 | 11110000 | | TSTIT | ,0360,,,TW | SEE IF ANY ERROR BIT SET (ZERO T IF NO) |
| 322. | 006410L | 11010011 | 11110101 | | BRA | IMASC2,TZ | |
| 323. | 006411L | 01010001 | 00000100 | | LDTI | B2 | YES. INCLUDE IT IN BITS SET |
| 324. | 006412L | 01010011 | 00000010 | IMASC2 | DOTI | ,OR,B1 | COMBINE READY WITH (MAYBE) THE ERROR BIT |
| 325. | 006413L | 01110011 | 11110001 | | DORR | TEMP1,OR,TEMP1 | SET RECEIVER & BREAK DETECTED BITS AS NEED |
| | 006414L | 01101111 | 11110001 | | | | |
| 326. | 006415L | | | IMASC1 | | | |
| 327. | 006415L | 00110001 | 00010111 | | TSTIP | ,B5+B4,ACUIN | PORT 3 OR 2 DSR/CD/RD/CTS SET? |
| | 006416L | 01000101 | 00110000 | | | | |
| 328. | 006417L | 11000010 | 00000110 | | BRA | IMASBSTS,FZ | YES |
| 329. | 006420L | 00110001 | 00010000 | | TSTIP | ,B6+B4,MODIN,TW | PORT 1 OR 0 DSR/CD/RD/CTS SET? |
| | 006421L | 01010101 | 01010000 | | | | |
| 330. | 006422L | 11000010 | 00000110 | | BRA | IMASBSTS,FZ | YES |
| 331. | 006423L | 11001111 | 00000101 | | BRA | IMASORZ | NO |
| 332. | | | | * | | | |
| 333. | 006424L | | | IMARDTA | | | |
| 334. | | | | . | | | |
| 335. | 006424L | 01010001 | 11101111 | | LDPI | MAH0H,SVCRCV>8 | ACCESS RECEIVER DATA (BUFFERED) |
| | 006425L | 00110111 | 11100000 | | | | |
| 336. | 006426L | 01110001 | 10111001 | | TSTIR | ,COMMPTS,COMMODE,CC,TW | |
| | 006427L | 01010101 | 00001111 | | | | |
| 337. | 006430L | 11010011 | 11010000 | | BRA | IMRNXPT,TZ | NOT A REAL PORT (SO ZERO) |
| 338. | 006431L | 01110001 | 11111001 | | LDTR | COMMODE | |
| 339. | 006432L | 01000101 | 00001100 | | BIT2ADR | SVCRCV-1 | |
| | 006433L | 11010011 | 11011111 | | | | |
| | 006434L | 01010100 | 00000001 | | | | |
| | 006435L | 01000101 | 00001100 | | | | |
| | 006436L | 11010011 | 11011111 | | | | |
| | 006437L | 01010001 | 00000100 | | | | |
| | 006440L | 01010010 | 01010011 | | | | |
| | 006441L | 00110111 | 11000000 | | | | |
| 340. | 006442L | 00110111 | 01000111 | | STB | SMR | |
| 341. | 006443L | 01110001 | 11111001 | | LDTR | COMMODE | |
| 342. | | | | | RPT | 4 | SELECT NECESSARY CONTROL BITS |
| 343. | 006444L | 00010111 | 10100010 | | SHIFT | SL | |
| 343. | 006445L | 00010111 | 10100010 | | SHIFT | SL | |
| 343. | 006446L | 00010111 | 10100010 | | SHIFT | SL | |
| 343. | 006447L | 00010111 | 10100010 | | SHIFT | SL | |
| 344. | 006450L | 01110011 | 11111001 | | DOTR | ,OR,COMMODE | THE RECEIVED & ERROR BITS |
| 345. | 006451L | 01010000 | 11111111 | | DOTI | ,XR,0377 | |
| 346. | 006452L | 01110101 | 11110111 | | DORR | RCVCTL,ND,RCVCTL | CLEAR PREVIOUS STATUS |

347. 006453L 01101111 11110111
 006454L 11010100 11010011
 006455L 11010111 00010001
 348. 006456L 00110001 00110110
 349. 006457L 00110111 10001111
 350. >006460L 01011001 11111111
 >006461L 11001111 11111111
 351.

MWAIT ,MEMPF6
 LDTP MDR AND GET THE RECEIVED DATA
 LDPT IMPO
 IMRNXP BRAX FETCH
 *

| | | | | | | |
|------|----------|----------|----------|---|----------------------------|---|
| 354. | | | * | | | |
| 355. | 006462L | | INPUT: | | | |
| 356. | | | . 3.70 | (101) IN | INPUT FROM 5500 BUS | |
| 357. | | | . 3.70 | (IMP 101) INR | (R) <- INBUS | |
| 358. | | | . ***** | | | |
| 359. | | | . NOTE: | INSTRUCTION FETCH TIME (APPROX. 2 MICRO-SEC.) INCLUDED IN COUNT FOR | | |
| 360. | | | . | TOTAL OF 5 MICRO-SEC. I/O TIMING OF THE INSTRUCTION. | | |
| 361. | | | . ***** | | | |
| 362. | | | | | | |
| 363. | 006462L | 00110001 | 11011100 | TSTIP | ,SWUSER,PSWI | |
| | 006463L | 01000101 | 00000100 | | | |
| 364. | 006464L | 11010010 | 00010011 | BRA | IVIOI6,FZ | CONTINUE ONLY IF IN PRIVIED MODE |
| 365. | 006465L | 01000101 | 00001000 | TSTIT | ,SWIDEV | |
| 366. | 006466L | 11000010 | 00101110 | BRA | IMAIN,FZ | |
| 367. | 006467L | 00110001 | 00010100 | INPUTX LDPP | SINS,INBUS,IMPO | GET INPUT DATA AND FAST ACKNOWLEDGE |
| | 006470L | 00110111 | 00101011 | | | |
| | 006471L | 00110111 | 10001111 | | | |
| 368. | 006472L | 00110001 | 00110001 | INPWI TSTIP | ,STIODR,STATUS | |
| | 006473L | 01000101 | 00000010 | | | |
| 369. | 006474L | 11010011 | 11000101 | BRA | INPWI,TZ | WAIT FOR ACK. TO MAKE ITSELF KNOWN |
| 370. | >006475L | 01011001 | 11111111 | FTCHIO BRAX | FETCHW | 'W' BECAUSE I/O DELAY TIMING NEEDS IT |
| | >006476L | 11001111 | 11111111 | | | |
| 371. | | | . | | | AS WELL AS EX ADR AND MIN MEMORY WRITES |
| 372. | | | * | | | |
| 373. | 006477L | | PIN: | | | |
| 374. | | | . 4.15 | (103) PIN | PARITY CHECKING INPUT | |
| 375. | | | . 4.15 | (IMP 103) PINR | (R) <- INBUS; PARITY CHECK | |
| 376. | | | . ***** | | | |
| 377. | | | . NOTE: | INSTRUCTION FETCH TIME (APPROX. 2 MICRO-SEC. INCLUDED IN COUNT FOR | | |
| 378. | | | . | TOTAL OF 5 MICRO-SEC. I/O TIMING OF THE INSTRUCTION. | | |
| 379. | | | . ***** | | | |
| 380. | | | | | | |
| 381. | 006477L | 00110001 | 11011100 | TSTIP | ,SWUSER,PSWI | |
| | 006500L | 01000101 | 00000100 | | | |
| 382. | 006501L | 11010010 | 00010011 | BRA | IVIOI6,FZ | DON'T CONTINUE UNLESS PRIVIED |
| 383. | 006502L | 01000101 | 00001000 | TSTIT | ,SWIDEV | |
| 384. | 006503L | 11010010 | 10111000 | BRA | PINERR,FZ | PIN'S GIVE PARITY FAULT ON 9462 |
| 385. | 006504L | 00110001 | 00110001 | TSTIP | ,STPFIN,STATUS | |
| | 006505L | 01000101 | 00000100 | | | |
| 386. | 006506L | 11010011 | 11001000 | BRA | INPUTX,TZ | NO PARITY FAULT, CONTINUE REGULAR INPUT |
| 387. | 006507L | 01010001 | 00000110 | PINERR LDTI | SVINP | USE PARITY INPUT ERROR VECTOR |
| 388. | >006510L | 01011001 | 11111111 | BRAX | SCLSTW | AND CALL SUPERVISOR ERROR ROUTINE |
| | >006511L | 11001111 | 11111111 | | | |
| 389. | | | . | | | PC CORRECT OR BACK UP IF IMP NON-ZERO |

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390.
391. 006512L
392.
393.
394.
395.
396. 006512L 00110001 11011111
      006513L 00110111 00100000
      006514L 00110111 00101100
397. 006515L 01010001 10101010
      006516L 00110111 11000000
      006517L 01010001 11101111
      006520L 00110111 11100000
398. 006521L 00110001 11011100
      006522L 01000101 00000100
399. 006523L 11010010 00010011
400. 006524L 01010101 11100111
      006525L 00110111 10001100
401. 006526L 00110001 11011111
      006527L 00110111 00100001
402. 006530L 01000000 01101001
403. 006531L 11010010 00100011
404. 006532L 01010001 00100000
      006533L 01101111 11111001
405.
406.
407.
408. 006534L 00010001 11111011
      006535L 01000101 10000000
409. 006536L 11010010 10011011
410. 006537L 01010001 10000000
      006540L 00000111 11111011
411. 006541L 01010001 00111111
      006542L 00110111 00100100
412. 006543L 01101111 11110011
413. 006544L 01010001 00001000
414. 006545L 11011111 10001010
415.
416. 006546L
417.
418.
419.
420. 006546L 00110001 11011111
      006547L 00110111 00100000
      006550L 00110111 00101100
421. 006551L 00110001 11011100
      006552L 01000101 00000100
422. 006553L 11010010 00010011
423. 006554L 01010001 11101111
424. 006555L 00110101 11011100
      006556L 00110111 10001100
425. 006557L 01000101 00001000

```

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+
EXADR:
. 9.40 ( 121) EX ADR      SELECT DEVICE (AND PUT IN STATUS MODE)
. 9.40 (IMP 121) EX ADR   (SEXADR) <- OUTBUS <- (R)

      LDPP      OTBUS,IMPI,SIOD  OUTPUT DATA AND START FIRST DELAY

      DLDPI     MARO,SEXADR

      TSTIP     ,SWUSER,PSWI     SHOULD I HAVE DONE THAT?

      BRA       IVIOL6,FZ
      DOPI      PSWO,ND,-1-SWSTD-T-SWIDEV  MARK IN STATUS & NON-IMA MODES

      LDPP      MDW,IMPI         OUTPUT ADDRESS TO ITS SAVE AREA

      TSTIT     XR,IMAADR        DID WE ADDRESS THE IMA?
      BRA       OUTWO,FZ
      LDRI      COMMODE,COMMNPS  SET ADDRESSED BUT NO PORT SELECTED

. **
. SET THE REAL TRANSMITTER & RECEIVER'S MODEM CONTROLS SO THAT THE SYSTEM
. WILL START INTERRUPTING CORRECTLY
      TSTIR     ,B7,TRNFCN      TURNED ON FIRST TIME?

      BRA       EXADML,FZ       YES, JUST ANOTHER SELECT
      LDRI      TRNFCN,B7       YES, REMEMBER IT

      LDPI      ACUOT,077       MP IS NOW ON, LINE LEFT MARKING

      EXADML    LDRT      TRNCHN  REMEMBER AS FIRST INTERRUPTS ARRIVE
               LDTI      SWIDEV
               BRA       PSWOR

*
EXSTAT:
. 9.05 ( 123) EX STATUS    PUT IN STATUS MODE
. 9.05 (IMP 123) EX STATUS  OUTBUS <- (R)

      LDPP      OTBUS,IMPI,SIOD  OUTPUT DATA AND START FIRST DELAY

      TSTIP     ,SWUSER,PSWI     SHOULD I HAVE DONE THAT?

      BRA       IVIOL6,FZ
      LDTI      -1-SWSTD-T
      PSWND     DOPP      PSWO,ND,PSWI  MARK IN STATUS MODE
               CLEAR TO CORRECT MODE

      TSTIT     ,SWIDEV

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| | | | | | | | |
|------|----------|----------|----------|---------|-----------|-----------------|-----------------------------------|
| 426. | 006560L | 11010011 | 00100011 | | BRA | OUTW0,TZ | |
| 427. | >006561L | 01011001 | 11111111 | | BRAX | FETCHI | |
| | >006562L | 11001111 | 11111111 | | | | |
| 428. | | | | * | | | |
| 429. | 006563L | | | EXDATA: | | | |
| 430. | | | | . 9.05 | (125) | EX DATA | PUT IN DATA MODE |
| 431. | | | | . 9.05 | (IMP 125) | EX DATA | OUTBUS <= (R) |
| 432. | | | | | | | |
| 433. | 006563L | 00110001 | 11011111 | | LDPP | OTBUS,IMPI,SIOD | OUTPUT DATA AND START FIRST DELAY |
| | 006564L | 00110111 | 00100000 | | | | |
| | 006565L | 00110111 | 00101100 | | | | |
| 434. | 006566L | 00110001 | 11011100 | | TSTIP | ,SWUSER,PSWI | SHOULD I HAVE DONE THAT? |
| | 006567L | 01000101 | 00000100 | | | | |
| 435. | 006570L | 11010010 | 00010011 | | BRA | IVIO16,FZ | |
| 436. | 006571L | 01010001 | 00010000 | | LDTI | SWSTDT | MARK IN DATA MODE |
| 437. | 006572L | 00110011 | 11011100 | PSWOR | DOPP | PSWO,OR,PSWI | SET CORRECT MODE STATE |
| | 006573L | 00110111 | 10001100 | | | | |
| 438. | 006574L | 01000101 | 00001000 | | TSTIT | ,SWIDEV | |
| 439. | 006575L | 11010011 | 00100011 | | BRA | OUTW0,TZ | |
| 440. | >006576L | 01011001 | 11111111 | | BRAX | FETCHW | (FETCHW FOR EX ADR) |
| | >006577L | 11001111 | 11111111 | | | | |


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441.
442. 006600L
443.
444.
445.
446. 006600L
447.
448.
449.
450. 006600L 00110001 11011111
      006601L 00110111 00100000
      006602L 00110111 00101100
451. 006603L 00110001 11011100
      006604L 01000101 00000100
452. 006605L 11010010 00010011
453. 006606L 01000101 00001000
454. 006607L 11010011 00100011
455. 006610L 01110001 10111001
      006611L 01000101 00001111
456. 006612L 11010011 11000010
457. 006613L 01000101 00001100
      006614L 11010011 01101110
      006615L 01010100 00000001
      006616L 01000101 00001100
      006617L 11010011 01101110
      006620L 01010001 00000100
      006621L 01010010 01010111
      006622L 00110111 11000000
458. 006623L 01010001 11101111
      006624L 00110111 11100000
459. 006625L 00110001 11011111
      006626L 00110111 00100001
460. 006627L 01110001 11111001
      006630L 01110011 11110101
      006631L 01101111 11110101
461. >006632L 01011001 11111111
      >006633L 11001111 11111111
462.
463. 006634L
464.
465.
466.
467. 006634L 00110001 11011111
      006635L 00110111 00100000
      006636L 00110111 00101100
468. 006637L 00110001 11011100
      006640L 01000101 00000100
469. 006641L 11010010 00010011
470. 006642L 01000101 00001000
471. 006643L 11010011 00100011
472. 006644L 00010111 10110010
473. 006645L 00110001 11011111

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+
OUTPUT:
. 9.05 (1xy: x=2,3: y ODD) EX COM OUTPUT TO 5500 BUS
. 9.05 (IMP 1xy) EXr COM OUTBUS <- (R)

EXWRITE:
. ( 127) EX WRITE WRITE DATA TO THE DEVICE
. (IMP 127) EXr WRITE

LDPP OTBUS,IMPI,SIOD OUTPUT DATA AND START ZEROth DELAY

TSTIP ,SWUSER,PSWI

BRA IVIOL6,FZ ONLY CONTINUE IF PRIVED
TSTIT ,SWIDEV
BRA OUTW0,TZ NOT SPECIAL, DO NORMAL I/O
EXMOUT: TSTIR ,COMMPTS,COMMODE,CC

BRA FTCHIO,TZ DO NOTHING FOR PORTS 4-7 (NON-EXISTANT)
BIT2ADR SVCTRn-1 POINT TO TRANSMITTER BUFFER POSITION

LDPI MAROH,SVCTRn>8

LDPP MDW,IMPI OUTPUT NEW DATA BYTE TO BE TRANSMITTED

DORRR TRNCTL,OR,TRNCTL,COMMODE SET THE BIT THAT DATA AVAILABLE

BRAX FETCHW

*
EXCOM3:
. ( 135) EX COM3 DO CONTROL STROBE 3
. (IMP 135) EXr COM3

LDPP OTBUS,IMPI,SIOD OUTPUT DATA AND START ZEROth DELAY

TSTIP ,SWUSER,PSWI

BRA IVIOL6,FZ ONLY CONTINUE IF PRIVED
TSTIT ,SWIDEV
BRA OUTW0,TZ NOT SPECIAL, DO NORMAL I/O
CCLR
DOTIP ,ND,07,IMPI SELECT LOWER 3 BITS

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| | | | | | | |
|------|----------|----------|----------|------------|--------------------|---------------------------------------|
| 474. | 006646L | 01010101 | 00000111 | | | |
| | 006647L | 01010010 | 01001101 | DORA | LINK,AC,EXC3B | |
| | 006650L | 01101111 | 11110000 | | | |
| 475. | 006651L | 01010001 | 00000001 | LDTI | 1 | SHIFT BIT INTO POSITION |
| 476. | 006652L | 11101111 | 00000000 | BRR | LINK | |
| 477. | 006653L | 11001110 | 11111111 | NOOP | | SET BIT 4 |
| 478. | 006654L | 11001110 | 11111111 | NOOP | | SET BIT 4 (COMMXP BIT) |
| 479. | 006655L | 11001110 | 11111111 | NOOP | | SET BIT 4 |
| 480. | 006656L | 00010111 | 10100010 | SHIFT | SL | SET BIT 4 |
| 481. | 006657L | 00010111 | 10100010 | SHIFT | SL | SET BIT 3 |
| 482. | 006660L | 00010111 | 10100010 | SHIFT | SL | SET BIT 2 (CIRCULAR SHIFT) |
| 483. | 006661L | 00010111 | 10100010 | SHIFT | SL | SET BIT 1 |
| 484. | 006662L | 01101111 | 11111001 | EXC3B LDRT | COMMODE | STORE BIT IN CORRECT POSITION |
| 485. | >006663L | 01011001 | 11111111 | BRAX | FETCH | |
| | >006664L | 11001111 | 11111111 | | | |
| 486. | | | | * | | |
| 487. | 006665L | | | EXCOM1: | | |
| 488. | | | | . | (131) EX COM1 | DO CONTROL STROBE 1 |
| 489. | | | | . | (IMP 131) EXr COM1 | |
| 490. | | | | | | |
| 491. | 006665L | 00110001 | 11011111 | LDPP | OTBUS,IMPI,SIOB | OUTPUT DATA AND START ZEROth DELAY |
| | 006666L | 00110111 | 00100000 | | | |
| | 006667L | 00110111 | 00101100 | | | |
| 492. | 006670L | 00110001 | 11011100 | TSTIP | ,SWUSER,PSWI | |
| | 006671L | 01000101 | 00000100 | | | |
| 493. | 006672L | 11010010 | 00010011 | BRA | IVIO16,FZ | ONLY CONTINUE IF PRIVED |
| 494. | 006673L | 01000101 | 00001000 | TSTIT | ,SWIDEV | |
| 495. | 006674L | 11010011 | 00100011 | BRA | OUTW0,TZ | DO NORMAL I/O |
| 496. | 006675L | 01110001 | 11111001 | TSTIR | ,COMMPTS,COMMODE | |
| | 006676L | 01000101 | 00001111 | | | |
| 497. | 006677L | 11010011 | 11000010 | BRA | FTCH10,TZ | DO NOTHING UNLESS PORTS 0..3 SELECTED |
| 498. | 006700L | 01010001 | 00110011 | BAL | LINK,EXCIMCLR | ASSUME DTR NOT SET |
| | 006701L | 01101111 | 11110000 | | | |
| 499. | 006702L | 00110001 | 11011111 | TSTIP | ,B4,IMPI | WAS THAT BIT SET? |
| | 006703L | 01000101 | 00010000 | | | |
| 500. | 006704L | 11010011 | 00111000 | BRA | EXCICHN,TZ | NO, WASN'T |
| 501. | 006705L | 01010001 | 00110000 | BAL | LINK,EXCIMSET | YES, IT WAS |
| | 006706L | 01101111 | 11110000 | | | |
| 502. | | | | . | | |
| 503. | 006707L | 01110001 | 11111001 | EXCICHN | TSTIR ,B2,COMMODE | CONVERT CHANNEL NO. TO BIT POSITION |
| | 006710L | 01000101 | 00000100 | | | |
| 504. | 006711L | 11010011 | 00110100 | BRA | EXCINT2,TZ | NOT CHANNEL 2 (ITS POSITION IS OK) |
| 505. | 006712L | 01010001 | 00010000 | LDTI | B4 | CH. 2'S BIT IN SPECIAL POSITION |
| 506. | 006713L | 11101111 | 00000000 | EXCINT2 | BRR LINK | NOW, SET OR CLEAR THAT BIT |
| 507. | | | | . | | |
| 508. | 006714L | 01010000 | 11111111 | EXCIMCLR | DOTI ,XR,0377 | CLEAR, INVERT BITS |
| 509. | 006715L | 00010101 | 11111011 | DOTR | ,ND,TRNFCN | SO CAN 'AND' THE BIT OUT |
| 510. | 006716L | 11011111 | 00101111 | BRA | EXCIMDO | SHOW THE RESULTS |
| 511. | | | | . | | |
| 512. | 006717L | 00010011 | 11111011 | EXCIMSET | DOTR ,OR,TRNFCN | SET, SO SET THE BIT |
| 513. | 006720L | 00000111 | 11111011 | EXCIMDO | LDRT TRNFCN | REMEMBER THE NEW STATE |
| 514. | 006721L | 00110111 | 00100101 | LDPT | SDLCMD | SHOW IT TO THE WORLD |

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515. >006722L 01011001 11111111
      >006723L 11001111 11111111
516.
517. 006724L
518.
519.
520. 006724L
521.
522.
523.
524. 006724L 00110001 11011111
      006725L 00110111 00100000
      006726L 00110111 00101100
525. 006727L 00110001 11011100
      006730L 01000101 00000100
526. 006731L 11010010 00010011
527. 006732L 01000101 00001000
528. 006733L 11010010 11000010
529. 006734L 00110001 00110001
      006735L 01000101 00000010
530. 006736L 11010011 00100011
531. 006737L 00110111 00101111
532. 006740L 00110001 00110001
      006741L 01000101 00000010
533. 006742L 11010011 00011111
534. 006743L 00110111 00101100
535. 006744L 00110001 00110001
      006745L 01000101 00000010
536. 006746L 11010011 00011011
537. 006747L 01000101 00001000
538. 006750L 11010011 11000010
539. 006751L 01010001 00001100
540. >006752L 01011001 11111111
      >006753L 11001111 11111111
541.
542. >006754L 01011001 11111111
      >006755L 11001111 11111111
543. >006756L 01011001 11111111
      >006757L 11001111 11111111
544.
545.
546. 006760L 11111111 11111111
547.
548. 001000
549. 006000
550. 006000
551.

```

BRAX FETCH AND DONE

*
EXCOM2:
 (133) EX COM2 DO CONTROL STROBE 2
 (IMP 133) EXr COM2
EXCOM4:
 (137) EX COM4 DO CONTROL STROBE 4
 (IMP 137) EXr COM4

LDPP OTBUS,IMPI,SIOD OUTPUT DATA AND START ZEROth DELAY

TSTIP ,SWUSER,PSWI

BRA IVIOL6,FZ ONLY CONTINUE IF PRIVED
TSTIT ,SWIDEV
BRA FTCHIO,FZ ** DO NOTHING WHERE NOTHING TO DO **
OUTW0 TSTIP ,STIODR,STATUS

BRA OUTW0,TZ DELAY 0 WAITING FOR DATA TO REACH DEVICE
STB SOTS GIVE COMMAND
OUTW1 TSTIP ,STIODR,STATUS

BRA OUTW1,TZ DELAY 1 WAITING FOR COMMAND TO GET THERE
STB SIOD EXTEND THE COMMAND DELAY FOR FINAL STEP
OUTW2 TSTIP ,STIODR,STATUS

BRA OUTW2,TZ DELAY 2 WAITING FOR PARITY TO RETURN
TSTIT ,STPFOU WAS THERE AN OUTPUT PARITY FAULT?
BRA FTCHIO,TZ NO!
LDTI SVOUTP YES, TELL SUPERVISOR THAT THERE WAS
BRAX SCLSTW

*
IVIOL6 BRAX IVIOLs

MEMPF6 BRAX MEMPFs

LIST -G
TABPAGE CDOXL
LIST G
CDOXLEN EQU \$-CDOXP "X"'S WERE "R"'S
USE CDOXL
SKIP CDOXLEN
END

*** ERRORS: D

① IMA SCLSTW TSTIP ,MCDIN, BTB,
BAA IMADSTS, FZ
BAA IMA SCLSTW

DATAPOINT CONFIDENTIAL INFORMATION - SEE PAGE 1

PAGE 28 PROC14/LIB:DR0.MLTI

MICRO-PROCESSOR MULTIPOINT COMM SUPPORT - HJS -
SATURDAY, AUGUST 7, 1982 -- 3:52:37 PM

07AUG82 15:52

| | | | 115 | 145 | 207 | 208 | 209 | 210 | 231 | 237 | 252 | 339 | 457 | 474 |
|--------|----------|-----|--------|-------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 010017 | AC | | 115 | 145 | 207 | 208 | 209 | 210 | 231 | 237 | 252 | 339 | 457 | 474 |
| 010017 | ACCTL | | *56:I | | | | | | | | | | | |
| 010015 | ACD | | *53:I | | | | | | | | | | | |
| 010017 | ACPH | | *55:I | 56:I | | | | | | | | | | |
| 010016 | ACPL | | *54:I | | | | | | | | | | | |
| | ACUIN | | 207 | 208 | 209 | 210 | 306 | 327 | | | | | | |
| | ACUOT | | 411 | | | | | | | | | | | |
| 010014 | APFRK | | *47:I | | | | | | | | | | | |
| 010013 | APFRP | | *46:I | | | | | | | | | | | |
| 010016 | APFTK | | *49:I | | | | | | | | | | | |
| 010015 | APFTP | | *48:I | | | | | | | | | | | |
| | B0 | | 51 | 279 | 317 | | | | | | | | | |
| | B1 | | 51 | 289 | 295 | 324 | | | | | | | | |
| | B2 | | 51 | 288 | 293 | 323 | 503 | | | | | | | |
| | B3 | | 51 | 71 | 293 | | | | | | | | | |
| | B4 | | 50 | 143 | 187 | 298 | 327 | 329 | 499 | 505 | | | | |
| | B5 | | 49 | 71 | 143 | 187 | 327 | | | | | | | |
| | B6 | | 71 | 301 | 329 | | | | | | | | | |
| | B7 | | 71 | 408 | 410 | | | | | | | | | |
| 006014 | BITOK | (M) | *115 | 115 | | | | | | | | | | |
| 006440 | BITOK | (M) | *339 | 339 | | | | | | | | | | |
| 006621 | BITOK | (M) | *457 | 457 | | | | | | | | | | |
| 020006 | BR | | *21:I | | | | | | | | | | | |
| 000100 | CAP55IO | | *121:I | 125:I | | | | | | | | | | |
| 000102 | CAPABILI | | *125:I | | | | | | | | | | | |
| 000000 | CAPAPF | | *118:I | 125:I | | | | | | | | | | |
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